74HC7540-Q100

Octal Schmitt trigger buffer/line driver; 3-state; inverting

Rev. 1 — 9 November 2023 Product data sheet

1. General description

The 74HC7540-Q100 is an 8-bit inverting buffer/line driver with Schmitt-trigger inputs and 3-state outputs. The device features two output enables ($\overline{OE}1$ and $\overline{OE}2$). A HIGH on $\overline{OE}n$ causes the outputs to assume a high-impedance OFF-state. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}. Schmitt trigger inputs transform slowly changing input signals into sharply defined jitter-free output signals.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Unlimited input rise and fall times
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Inverting outputs
- CMOS input levels
- Complies with JEDEC standards
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC7540D-Q100	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1

nexperia

4. Functional diagram

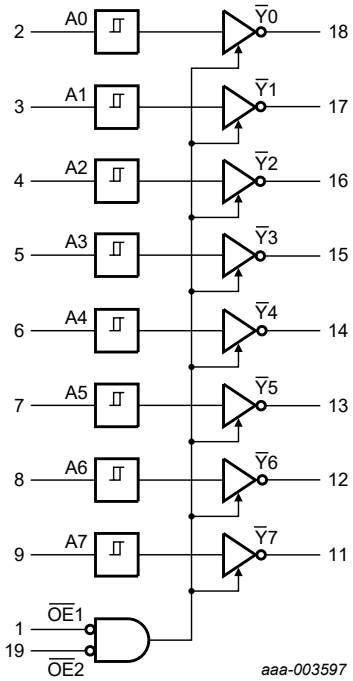


Fig. 1. Logic symbol

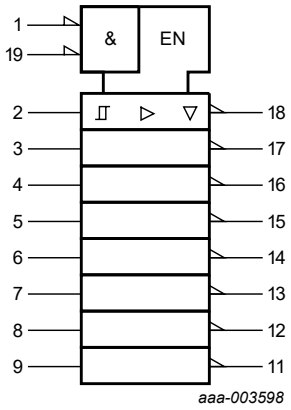
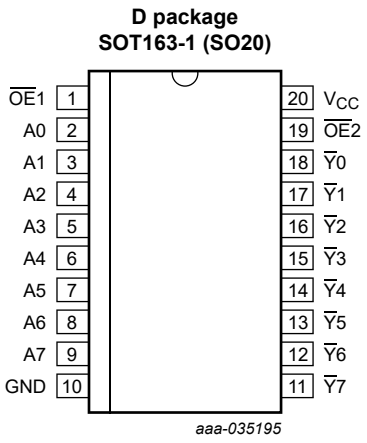


Fig. 2. IEC logic symbol

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}1$	1	output enable input (active LOW)
A0, A1, A2, A3, A4, A5, A6, A7	2, 3, 4, 5, 6, 7, 8, 9	data input
GND	10	ground (0 V)
$\overline{Y}0$, $\overline{Y}1$, $\overline{Y}2$, $\overline{Y}3$, $\overline{Y}4$, $\overline{Y}5$, $\overline{Y}6$, $\overline{Y}7$	18, 17, 16, 15, 14, 13, 12, 11	data output
$\overline{OE}2$	19	output enable input (active LOW)
V_{CC}	20	supply voltage

6. Functional description

Table 3. Functional table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control		Input	Output
$\overline{OE}1$	**$\overline{OE}2$**	**An**	**$\overline{Y}n$**
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V		-	±35	mA
I_{CC}	supply current			-	70	mA
I_{GND}	ground current			-70	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation		[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT163-1 (SO20) package: P_{tot} derates linearly with 12.3 mW/K above 109 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}								
		I_O = -20 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -20 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -20 µA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = -6.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = -7.8 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}								
		I_O = 20 µA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 6.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 7.8 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{OZ}	OFF-state output current	$V_I = V_{T+}$ or V_{T-}; V_{CC} = 6.0 V; $V_O = V_{CC}$ or GND	-	-	±0.5	-	±5.0	-	±10	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; C_L = 50 pF; for test circuit see Fig. 5.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	An to $\overline{Y}$n; see Fig. 3 [1]								
		V_{CC} = 2.0 V	-	39	120	-	150	-	180	ns
		V_{CC} = 4.5 V	-	14	24	-	30	-	36	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	11	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	11	20	-	26	-	31	ns
t_{en}	enable time	$\overline{OE}$n to $\overline{Y}$n; see Fig. 4 [1]								
		V_{CC} = 2.0 V	-	41	150	-	190	-	225	ns
		V_{CC} = 4.5 V	-	15	30	-	38	-	45	ns
		V_{CC} = 6.0 V	-	12	26	-	33	-	38	ns
t_{dis}	disable time	$\overline{OE}$n to $\overline{Y}$n; see Fig. 4 [1]								
		V_{CC} = 2.0 V	-	52	150	-	190	-	225	ns
		V_{CC} = 4.5 V	-	19	30	-	38	-	45	ns
		V_{CC} = 6.0 V	-	15	26	-	33	-	38	ns
t_t	transition time	see Fig. 3 [2]								
		V_{CC} = 2.0 V	-	14	60	-	75	-	90	ns
		V_{CC} = 4.5 V	-	5	12	-	15	-	18	ns
		V_{CC} = 6.0 V	-	4	10	-	13	-	15	ns
C_{PD}	power dissipation capacitance	per package; V_I = GND to V_{CC} [3]	-	29	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}; t_{en} is the same as t_{PZL} and t_{PZH}; t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[2] t_t is the same as t_{THL} and t_{TLH}.

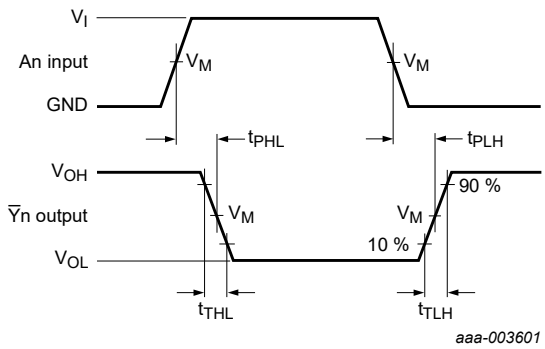
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF;

V_{CC} = supply voltage in V; N = number of inputs switching; $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

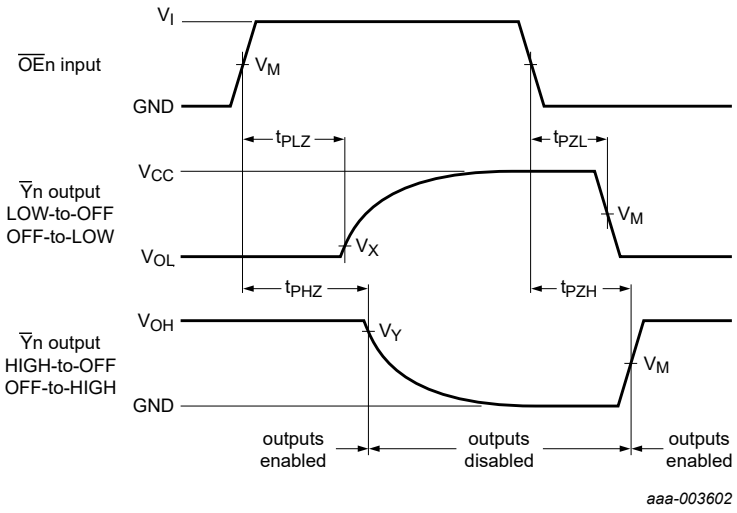
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 3. Input to output propagation delays



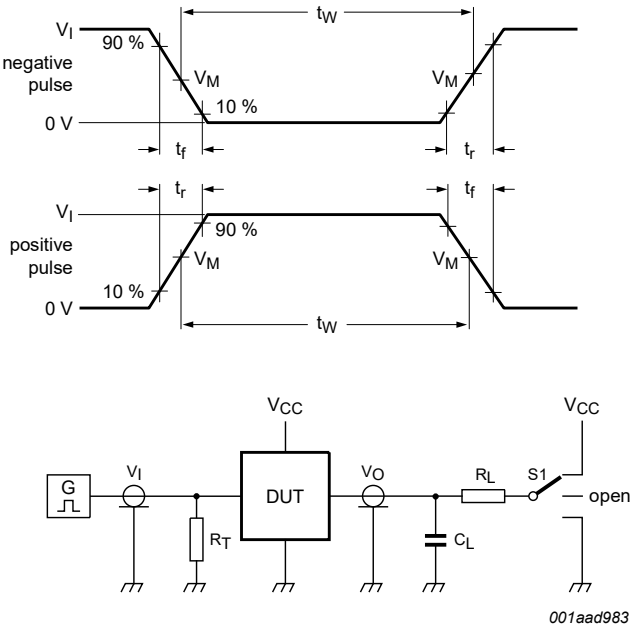
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 4. 3-state enable and disable times

Table 8. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
0.5 × V_{CC}	0.5 × V_{CC}	0.1 × V_{CC}	0.9 × V_{CC}



Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistance;

S1 = Test selection switch.

Fig. 5. Test circuit for measuring switching times

Table 9. Test data

Input		Load		S1 position		
V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

11. Transfer characteristics

Table 10. Transfer characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); see Fig. 6 and Fig. 7.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{T+}	positive-going threshold voltage	V_{CC} = 2.0 V	-	-	1.5	-	1.5	-	1.5	V
		V_{CC} = 4.5 V	-	-	3.15	-	3.15	-	3.15	V
		V_{CC} = 6.0 V	-	-	4.2	-	4.2	-	4.2	V
V_{T-}	negative-going threshold voltage	V_{CC} = 2.0 V	0.3	-	-	0.3	-	0.3	-	V
		V_{CC} = 4.5 V	1.35	-	-	1.35	-	1.35	-	V
		V_{CC} = 6.0 V	1.8	-	-	1.8	-	1.8	-	V
V_H	hysteresis voltage	V_{CC} = 2.0 V	0.1	0.20	-	0.1	-	0.1	-	V
		V_{CC} = 4.5 V	0.25	0.40	-	0.25	-	0.25	-	V
		V_{CC} = 6.0 V	0.3	0.5	-	0.3	-	0.3	-	V

11.1. Transfer characteristics waveforms

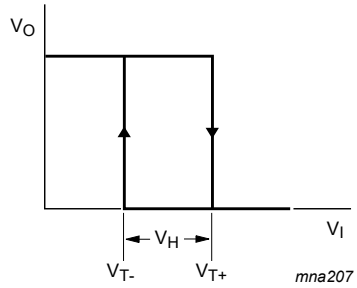


Fig. 6. Transfer characteristics

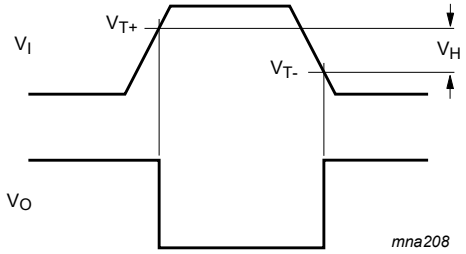
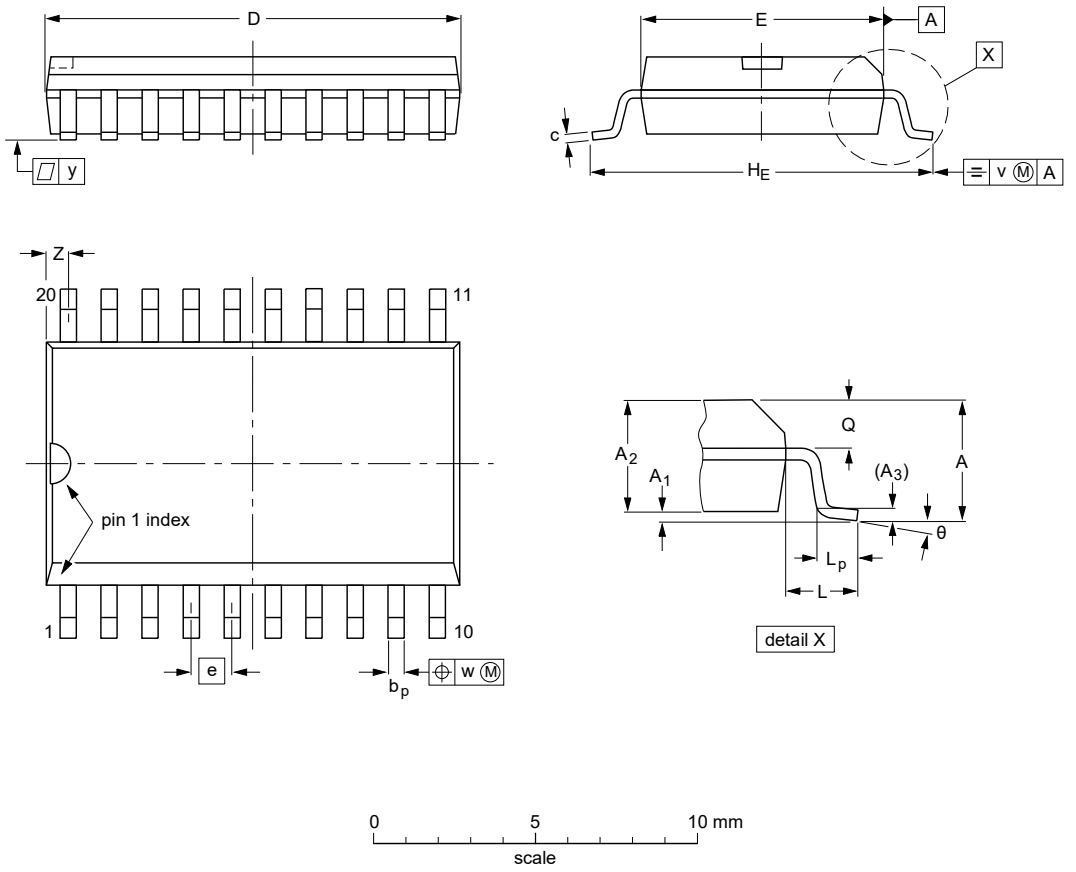


Fig. 7. Transfer characteristics definitions

12. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig. 8. Package outline SOT163-1 (SO20)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC7540_Q100 v.1	20231109	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 9 November 2023